

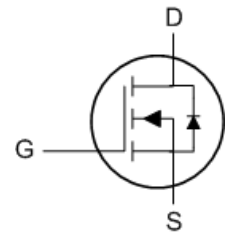
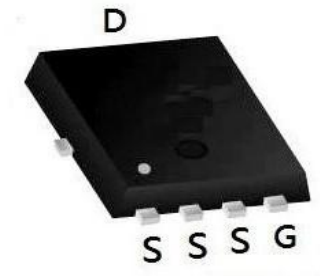
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology


Product Summary

BVDSS	RDSON	ID
20V	2.2mΩ	100A

Description

The XXW100N02F is the high cell density trench N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The XXW100N02F meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PDFN5060-8L Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	100	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	63	A
I_{DM}	Pulsed Drain Current ²	400	A
EAS	Single Pulse Avalanche Energy ³	306	mJ
I_{AS}	Avalanche Current	---	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	69	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	---	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	1.8	$^{\circ}C/W$

Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	---	---	V/ $^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=17.5A$	---	---	---	m Ω
		$V_{GS}=4.5V$, $I_D=17.5A$	---	2.2	2.9	
		$V_{GS}=2.5V$, $I_D=13A$	---	2.7	3.5	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	0.5	---	1	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	---	---	mV/ $^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=20V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=20V$, $V_{GS}=0V$, $T_J=125^{\circ}\text{C}$	---	---	100	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 12V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=17.5A$	---	88	---	S
Q_g	Total Gate Charge	$V_{DS}=10V$, $V_{GS}=4.5V$, $I_D=17.5A$	---	70	---	nC
Q_{gs}	Gate-Source Charge		---	10	---	
Q_{gd}	Gate-Drain Charge		---	14	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DS}=10V$, $V_{GS}=4.5V$, $R_G=3\Omega$, $R_L=0.5\Omega$	---	8	---	ns
T_r	Rise Time		---	20	---	
$T_{d(off)}$	Turn-Off Delay Time		---	75	---	
T_f	Fall Time		---	82	---	
C_{iss}	Input Capacitance	$V_{DS}=10V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	5670	---	pF
C_{oss}	Output Capacitance		---	460	---	
C_{rss}	Reverse Transfer Capacitance		---	416	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	100	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=21A$, $T_J=25^{\circ}\text{C}$	---	---	1	V
t_{rr}	Reverse Recovery Time	$I_F=17.5A$, $di/dt=100A/\mu s$,	---	15	---	nS
Q_{rr}	Reverse Recovery Charge	$T_J=25^{\circ}\text{C}$	---	6	---	nC

Note :

- 1..Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2.EAS condition: $T_J=25^{\circ}\text{C}$, $V_{DD}=10V$, $V_G=10V$, $R_G=25\Omega$, $L=0.5\text{mH}$.
- 3.Repetitive Rating: Pulse width limited by maximum junction temperature.e.

Typical Electrical And Thermal Characteristics (Curves)

Figure 1. Output Characteristics

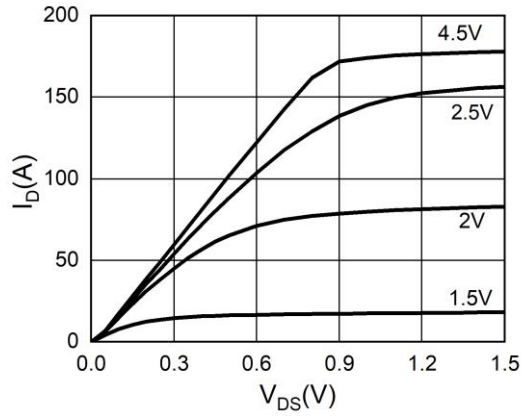


Figure 2. Transfer Characteristics

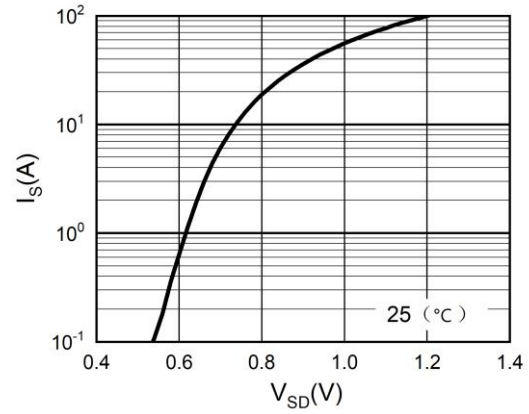


Figure 3. Power Dissipation

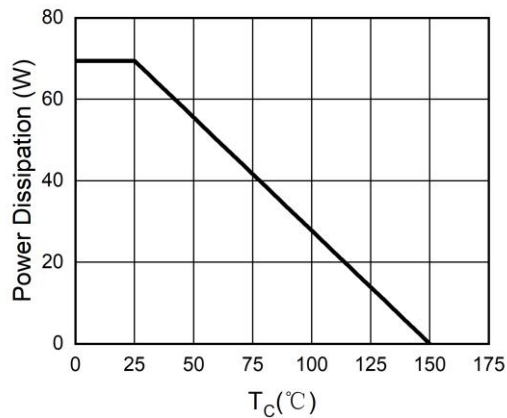


Figure 4. Drain Current

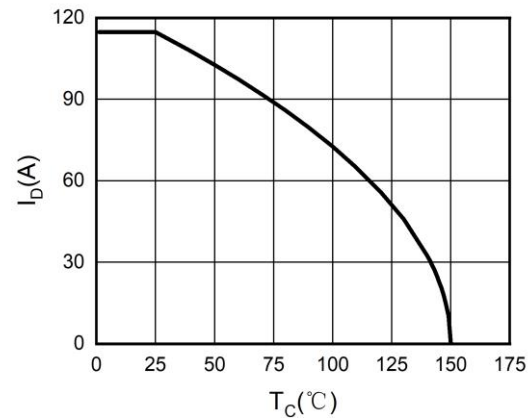


Figure 5. BV_{DSS} vs Junction Temperature

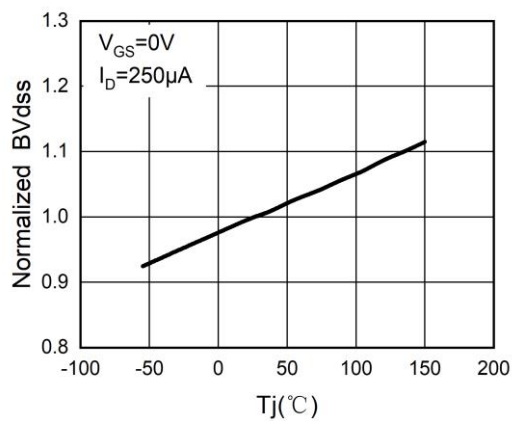
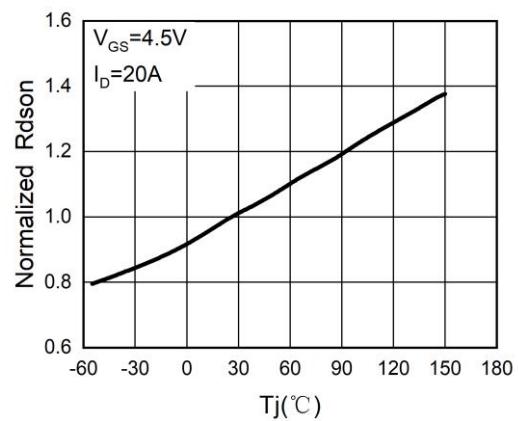


Figure 6. $R_{DS(ON)}$ vs Junction Temperature



Typical Electrical And Thermal Characteristics (Curves)

Figure 7. Gate Charge Waveforms

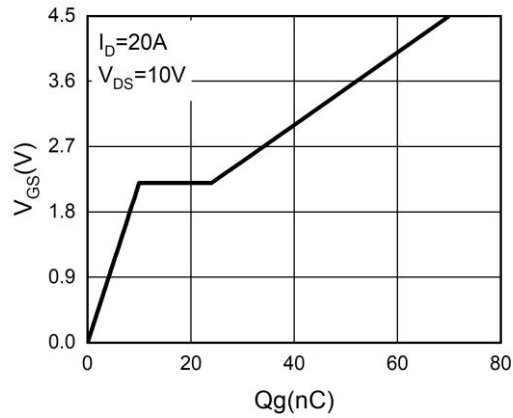


Figure 8. Capacitance

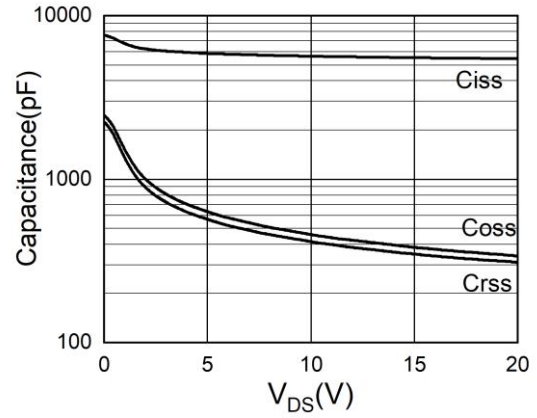


Figure 9. Body-Diode Characteristics

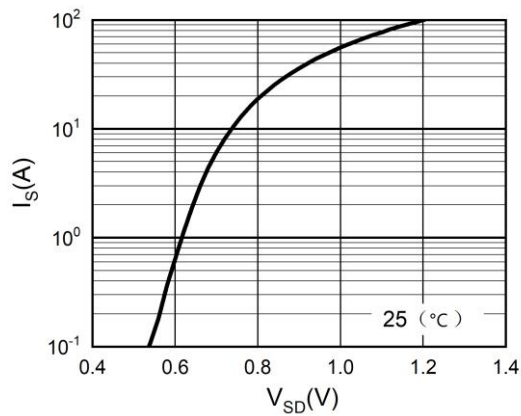
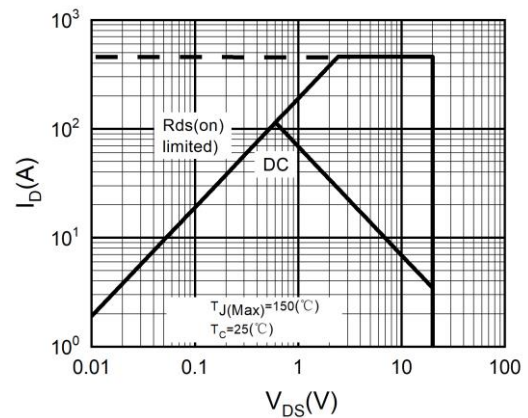


Figure 10. Maximum Safe Operating Area



Test Circuit

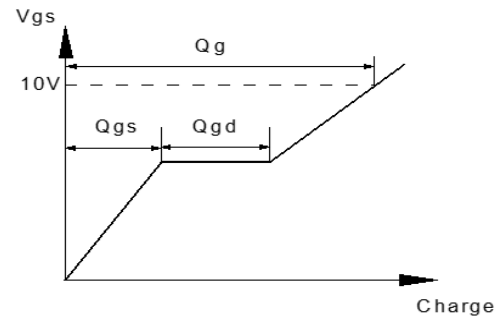
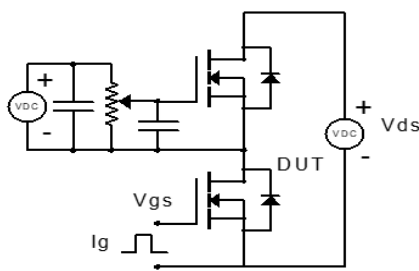


Figure 1: Gate Charge Test Circuit & Waveform

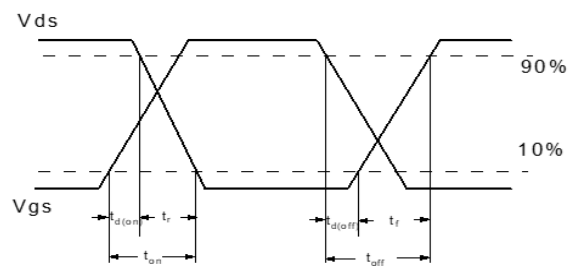
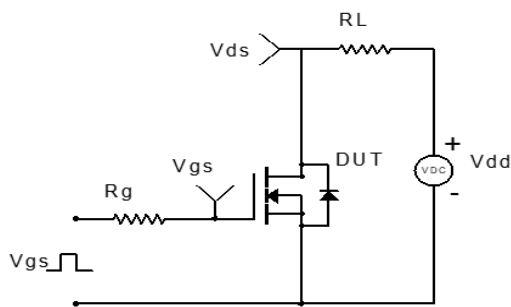


Figure 2: Resistive Switching Test Circuit & Waveform

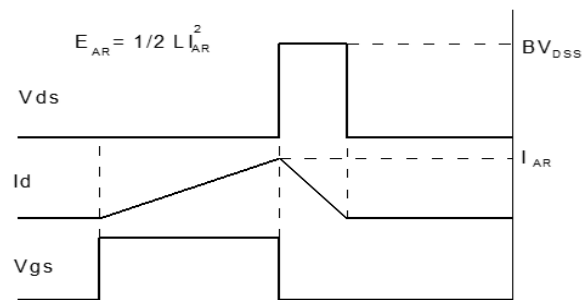
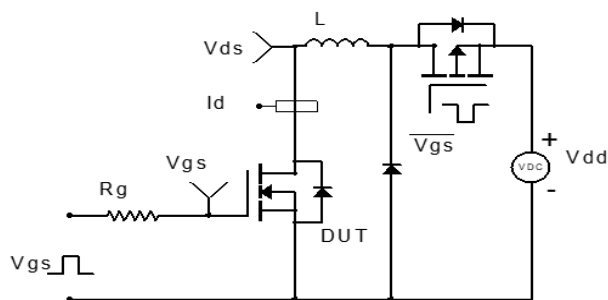


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

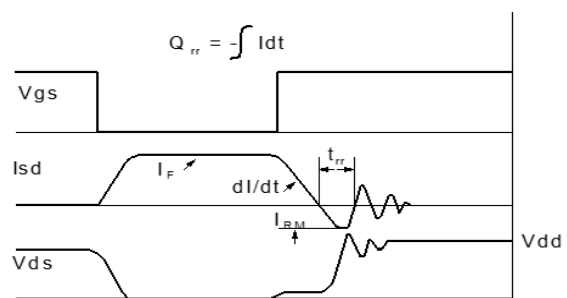
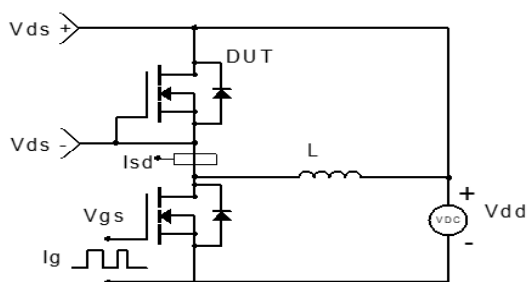
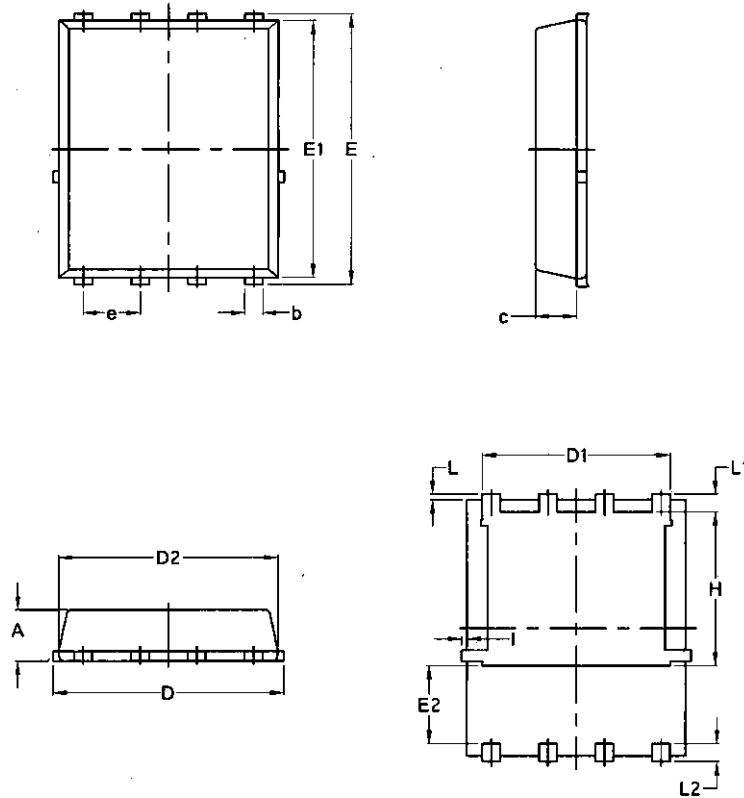


Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data-PDFN5060-8L-Single


Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070